Notice of Allowability	Application No.	Applicant(s)	
	10/815,492	ELDIN ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/20/06*.

2. ☒ The allowed claim(s) is/are *2-16 and 18-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *11/30/06* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Keith Chanroo on 11/30/06.

The application has been amended as follows:

As per claim 10:

A method of isolating a fault on a line segment of a switch matrix comprising: generating a first route between an input of the switch matrix and an output of the switch matrix through a first programmable interconnect point on the line segment and through a first adjacent programmable interconnect point; configuring the first route in the switch matrix; applying a first test vector at the input, the first test vector comprising a first series of first digital test values followed by a second series of second digital test values followed by a third series of the first digital test values; measuring first test data at the output; storing the first test data and at least a portion of the first route; generating a second route between the input and the output through the first programmable interconnect point on the line segment and through a second adjacent programmable interconnect point; configuring the second route in the switch matrix; applying a second test vector at the input; measuring second test data at the output; storing the second test data and at least a portion of the second route; and comparing the first test data

and the second test data against a layout schematic of a programmable logic device so as to locate the fault on the failed line segment.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

The present invention pertains to a circuit and method for testing programmable interconnecting points of the Field Programmable Gate Arrays (FPGA).

The claimed invention recites features such as: a method of isolating a fault on a line segment of a switch matrix comprising: generating a first route between an input of the switch matrix and an output of the switch matrix through a first programmable interconnect point on the line segment and through a first adjacent programmable interconnect point; configuring the first route in the switch matrix; applying a first test vector at the input; measuring first test data at the output; storing the first test data and at least a portion of the first route; generating a second route between the input and the output through the first programmable interconnect point on the line segment and through a second adjacent programmable interconnect point, configuring the second route in the switch matrix; applying a second test vector at the input; measuring second test data at the output; and comparing the first test data and the second test data against a layout schematic of a programmable logic device so as to locate the fault on the failed line segment.

The prior art of record Dastidar et al. US Patent no. 7,024,327 B1, teaches generating routes and performing a series of tests to detect the presence of any

manufacturing detects. Merely detecting the defect occurs along a line segment somewhere along that path. Dastidar et al. does not anticipate or render obvious isolating the specific programmable point, where the defect occurs. Further, Dastidar et al. does not anticipate or render obvious generating the routes specifically between certain interconnection programmable points and the respective adjacent interconnection programmable points.

The prior arts of record fail to anticipate or render obvious the present invention. Therefore claims 2-16 & 18-25 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S.S

Saqib Siddiqui
Art Unit 2138
11/30/2006

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